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Analog Front-End Design for Biomedical Signal Acquisition Systems

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Abstract This manuscript contains a brief overview of the work being carried out by the author under the aegis of Visvesvaraya Young Faculty Research Fellowship awarded to him by the Ministry of Electronics and Information Technology (MeitY), India.

Keywords Analog Front-End Design · Biomedical Signal Acquisition · CMOS · OTA · Subthreshold design · Ultra-low g_m

1 Overall Goals

The overall goal of the research work is twofold. A low power analog building block, specifically an ultra-low transconductance Operational Transconductance Amplifier (OTA), is to be designed. The OTA is then to be used in the design of an ultra-low power, low-noise, analog front-ends for physiological signal acquisition.

2 Context and Research Aims

Considering that the real world remains analog while signal processing becomes more and more digital, analog front-ends (AFE) are required for acquisition of analog signals and process them appropriately for use by subsequent digital processing stages. One specific scenario is where physiological signals from human body, for example signals from the heart i.e. electrocardiogram (ECG), brain i.e. electroencephalogram (EEG), eyes i.e. electrooculograph (EOG) etc., need to be acquired. Advancements in physiological signal acquisition techniques dictate the need for designing smaller and ultra low-power circuits targeted towards implantable devices. It is thus imperative to first have a basic analog building block which offers such capabilities. Opamp – the workhorse of analog industry, is not suitable for these applications because of the fact that opamp-RC implementations of most analog filters tend to have large valued resistors and capacitors (when designed for low frequencies corresponding to biomedical signals like ECG, EEG, EOG, etc.). The OTA provides a better alternative in the sense that $g_m - C$ filters are inherently resistor-less, tunable and could be fabricated on ultra-small chip areas if the OTA transconductance could be made very small, as that would necessitate smaller capacitors for the same cut-off frequencies. Another major problem for the acquisition of bio-medical signals is power-line interference, *i.e.* noise due to AC mains (50 Hz in countries like India,60 Hz in others). Power-line interference usually occurs through electrode cables, electrical devices etc. and needs to be eliminated before any subsequent processing.

A typical EEG signal can have the following components: δ-wave (0.5–4Hz; 20–100μV), θ-wave (4–8Hz; 20–70μV), α-wave (8–13Hz; 20–100μV), β-wave (13–40Hz; 5–20μV). Usually EEG signals are captured in a noisy environment where 50Hz noise is the strongest source of noise and may even make the EEG signal undetectable. Since the power-line interference is very near to the frequency band of $\beta-$wave, generally very high-order low-pass filter is needed to eliminate it. An alternative approach is to use a low-pass notch filter, which provides low-pass characteristics for out-of-band frequency noises and high-attenuation to the 50 Hz power-line frequency.

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Table 1 Typical amplitude and frequency ranges of physiological signals

	Amplitude Range (mV)	Frequency Range (Hz)
ECG	0.05 – 3	0.01 – 300
EEG	0.001 – 1	0.1 – 100
EOG	0.00 – 0.3	0.1 – 10
EMG	0.001 – 1000	50 – 3000

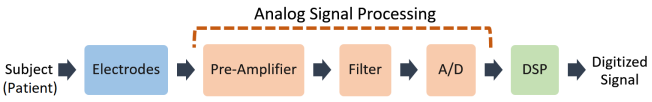

Fig. 1 Block diagram for Biomedical Signal Acquisition

This research therefore endeavors to add to the existing knowledge on two fronts. Firstly, the design of ultra-low transconductance OTAs, and secondly, the design of an ultra-low power analog front-end for physiological signal acquisition of the type shown in Fig 1.

3 Importance as a technical problem

The importance of real-time physiological signal monitoring cannot be overstated. Ever increasing population puts an escalating strain on medical facilities. Rapid increase in the number of cases of chronic diseases has made it non-negotiable to move to a proactive and prevention oriented approach, wherein continuous (and possibly discreet) sensing of body signals through wearable and implantable devices is required. Apart from processed locally , these signals can be remotely monitored and recorded to generate a medical history for subsequent analysis. Such acquisition devices are required to be small in size and (ideally) should not interfere with the normal body functioning and movement.

Circuits for acquiring such low-frequency signals require very large resistor and capacitor values, and take large on-chip area. However, design of implantable devices dictate need for smaller area. Also, the relatively small voltage signals are highly prone to picking noise from electrodes, power supplies and other sources. Another pertinent point of interest is the adoption of low power techniques to reduce heat dissipation to prevent thermal damage to tissues surrounding the implanted device. Low power, low voltage design also avoids use of bulky batteries, extends battery life and prevents the inconvenience of frequent battery replacement.

4 State of the Art

Zhu et al. presented a low-power AFE for Wireless Body Area Networks [14]. It consists of a chopped capacitively coupled instrumentation amplifier, switched capacitor filter and a successive approximation ADC. This AFE consumes 1.3μW and achieves a bandwidth of 0.5-250 Hz, CMRR of 95dB and input impedance of 48 MΩ. Wang et al. presented a fifth order fully differential CMOS low-pass notch filter with high interference rejection [11]. The filter has a bandwidth of 47.7 Hz, covering the EEG frequencies from 1 to 40 Hz with a notch of 73.2 dB at the 60 Hz powerline frequency. Yener et al. presented a memristor-based second order Sallen-Key band-pass filter and its application to EEG processing [13]. Ranjan et al. presented a new approach to the design of a comb filter wherein the use of a current conveyor is proposed to eliminate the undesired harmonic interference from the biomedical signal [8]. Tiwari and Sahu presented a low-noise filter for biomedical signals [10]. The fifth-order elliptical filter designed using OTA-C method is used to acquire biopotential signal in range of 40 Hz. The circuit was designed in 250 nm technology with 2.5 volt power supply. Bandwidth and noise of the filter are 38 Hz and 3.36$\mu V/\sqrt{Hz}$ respectively. Sinha et al. presented a 22nm CMOS AFE for biomedical applications [9]. This circuit is capable of reading out biomedical signals in the range of 0.01 Hz to 300 Hz in frequency, while rejecting power-line frequency of 50/60Hz. The OTA designed has a very low transconductance, which is programmable from 1.069nA/V to 2.114 nA/V. The power consumption of the entire AFE was found to be 11.34 nW at $\pm$0.95V supply. Mahmoud et al. presented an OTA-C low pass filter for a portable ECG system [5]. The filter provides a third harmonic distortion (HD3) of 53.5 dB for 100 mV p-p @50 Hz sinusoidal input, input referred noise spectral density of 120$\mu V_{rms}/\sqrt{Hz}$, total power consumption of 30μW, and a bandwidth of 243 Hz. Mahmoud et al. presented another OTA-C notch filter for ECG system [6]. A six order cascaded filter is utilized to reduce the effect of the power line interference at 50/60 Hz. The circuit was designed in 0.25 μm technology and operated with $\pm$0.8 V voltage supply. Chen et. al. recently proposed an extremely low-power, low-noise AFE for ECG and EEG applications [3], which is based on a high-pass, low-noise amplifier coupled with an inverter-based Sigma-Delta modulator. Results are provided for 0.13 μm CMOS technology, and show that for a 0.6 V power supply, the input referred noise is 3.976 μV_{rms} with 8.4 μW power consumption. Kosari et. al. presented an AFE for ECG signal acquisition and diagnosis of arrhythmia [4]. Their circuit uses aggressive voltage scaling to satisfy both the low power consumption and low input-referred noise requirements of ECG signal acquisition systems. The front-end was implemented in a 130 nm CMOS process using a 0.5 V supply, and provides a tunable mid-band gain from

$$V_{OUT} = \frac{s^n V_0 + a_{n-1}s^{n-1}V_1 + a_{n-2}s^{n-2}V_2 + \ldots + a_0 s^0 V_n}{s^n + a_{n-1}s^{n-1} + a_{n-2}s^{n-2} + \ldots + a_0 s^0} \quad \texttt{where} \quad a_k = \prod_{i=1}^{n-k} \frac{g_i}{C_i}; \quad k = 0, 1, 2, \ldots, (n-1) \tag{1}$$

31–52 dB while consuming 68 nW. Xu et. al. presented a 1.2 V, 36 μW AFE for multiple-mode acquisition [12] employing a reconfigurable preamplifier, a current generator, and a mixed signal processing unit, with five acquisition modes. The most significant characteristic of the circuit is its ability to interface with voltage-, current-, and light-sensors, and therefore the ability to measure galvanic skin response, electrocardiograph, *etc.*

5 Results

This section contains the results of the research work obtained thus far, and an outline for further endeavors over the short (1 year) and long (3 year) future horizons.

5.1 Results achieved so far

The initial research efforts have been focused on the design of a suitable analog building block for use in the low-power low-noise front-end. Some efforts have also been directed towards the design of one component (the noise rejection filter) of the analog front-end.

Design of Ultra-Low Transconductance OTA
CMOS OTAs designed with transistors working in strong inversion typically have g_m in the $\mu A/V$ regime. However, an OTA where all transistors are constrained to operate in weak inversion can be expected to yield significantly lower g_m values. This is the first objective of this work: to design an ultra-low g_m weak-inversion based CMOS OTA where all the constituent MOSFETs are operating in the subtheshold region of operation. Presently, the g_m/I_D design methodology appears to be the most promising technique available for the design of very-low power, ultra-low transconductance OTAs, and the same has been applied to the design of a Subthreshold CMOS OTA capable of exhibiting very low g_m values. The proposed low transconductance OTA circuit employs current division and current cancellation technique, and is shown in Fig. 2. The complete design process for the OTA appears in [1].

The performance of low transconductance OTA given in Fig. 2 was analysed in HSPICE using 180nm CMOS level 49 PTM model. For simulation purposes, bias voltages V_{bias1} and V_{bias2} is taken as 0.6V, supply voltages V_{DD} and V_{SS} were kept at $\pm$0.9V, and transistor dimensions are shown in Table 2. It was observed that

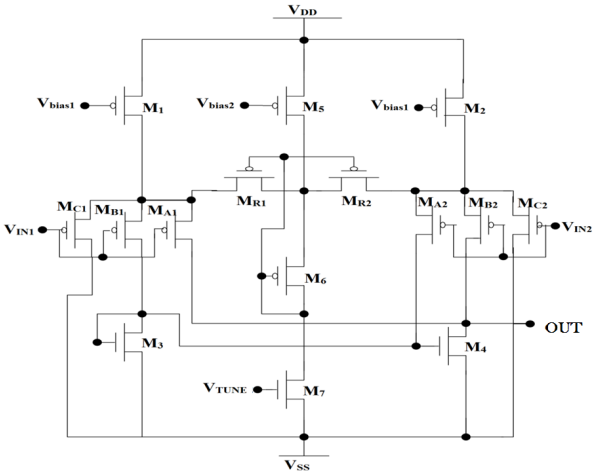

Fig. 2 CMOS implementation of the Subthreshold Ultra-Low g_m OTA

Table 2 Aspect ratios of transistors in Fig. 2

MOS	W(μm)	L(μm)	MOS	W(μm)	L(μm)
M1	100	0.18	MR1	2.06	0.18
M5	100	0.18	MR2	2.06	0.18
M2	20	0.18	M6	5.9	0.18
MC1	21.3	0.18	M3	6.6	0.18
MC2	21.3	0.18	M4	6.6	0.18
MB1	0.96	0.18	M7	1.48	0.18
MB2	0.96	0.18	MA1,2	2.06	0.18

as the value of V_{TUNE} was varied from $-$590mV to $-$630mV, the transconductance g_m varied from 1.36 nA/V to 5.59 nA/V which is sufficiently low for the required analog front-end design.

Design of Compact Ultra-Low Power Analog Front-End
Initially, the design of Power-Supply Noise Rejection Notch Filter as a component of the overall analog front-end was considered. Toward that end, three different OTA-C notch circuits were proposed [1,2].

Fig. 3 presents the three notch designs. The transfer function for the circuit of Fig. 3(a) is provided in (1).

For the circuit in Fig. 3(b) notch frequency of the OTA-C filter can be estimated as

$$f_1 = \frac{g_{m_{OTA}}}{2\pi\sqrt{C_{L2}C_2}} \tag{2}$$

Apart from the frequency above, the circuit of Fig. 3(c) exhibits another notch frequency given by

$$f_2 = \frac{g_{m_{OTA}}}{2\pi\sqrt{C_{L4}C_4}} \tag{3}$$

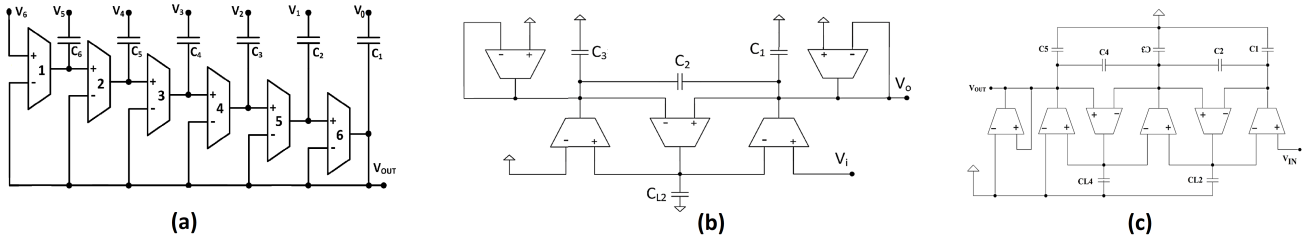

Fig. 3 Proposed notch filters based on the Subthreshold Ultra-Low g_m OTA

Comparison of the propsed AFEs with existing works
A performance comparison of the proposed notch circuits with existing CMOS notch filters was also performed, and the results of this comparison are presented in Table 3 and Table 4, from where it can be seen that the proposed circuits indeed provide improved characteristics over their existing counterpart [7].

5.2 Results expected in 1-year horizon

Design of Ultra-Low Transconductance OTA
In the next one year, it is expected that the design of a very-low power, ultra-low g_m (preferably in the range of pA/V) shall be finalized and extensively tested through computer simulations. It is envisioned that the final design would be better than the OTAs available in the technical literature in terms of transconductance (lower) and power consumption (lower).

Design of Compact Ultra-Low Power Analog Front-End
In the next one year, it is expected that the design of a low-power, low-noise pre-amplifier shall also be finalized, and verified at the simulation level. The design shall be evaluated against the available solutions and if needed be reiterated to better the performance.

Table 3 Comparison of the circuit of Fig. 3(a) with existing CMOS counterparts

Parameters	This work	[6]
OTA type	Current division and cancellation design	Fully balanced programmable OTA
Notch filter type	Canonical filter	Cascaded filter
Technology (μm)	0.18	0.25
No. of OTAs	6	27
No. of transistors per OTA	15	26
Notch @ 50Hz(dB)	28	37
Stopband noise ($\mu Vrms/\sqrt{Hz}$)	49	33
Passband noise (m $Vrms/\sqrt{Hz}$)	1.8	1
THD (%)	<2	Not given
Power Consumption (W)	9μ	31μ (for 1 block)

Table 4 Comparison of the circuit of Fig. 3(b, c) with existing CMOS counterparts

Parameters	This Work		[7]
	3rd order	5th order	5th order
Technology (μm)	0.18	0.18	0.35
Power Supplies (V)	$\pm$0.9	$\pm$0.9	$\pm$1.5
Order	3	5	5
Transconductance (nA/V)	1.36	1.36	3
No of OTA used	5	6	6
Capacitances values (pF)	1 to 6	1 to 6	1 to 15
Passband attenuation (dB)	-4	-4.7	-1
Stopband attenuation (dB)	-50	-44.8	-40
Bandwidth (Hz)	22	36	37
Notch@50Hz	-68	-66	-66
THD @vin of 8Hz and 5m$V_{p\text{-}p}$ (%)	1.7	0.6	0.326
Power consumption (W)	6μ	12μ	11μ

5.3 Results expected in 3-year horizon

Design of Compact Ultra-Low Power Analog Front-End
For the 3-year horizon, it is envisaged that the research work shall deliver a complete AFE with all the following modules fully designed and tested: pre-amplifier, filter, and A/D converter. As discussed before, the pre-amplifier should be a low-noise amplifier capable of suitably amplifying the physiological analog signal while removing noise present in the signal, and at the same time should not add any noise of its own. The filter(s) would comprise of a low-pass filter (to select the low-frequency bands of interest) and a notch filter (to remove the powerline frequency noise component present in the acquired signal). Further, an ultra-low power ADC capable of real-time conversion of the analog signal to its digital equivalent shall also be designed, thereby completing the design of the analog front-end.

6 Major publications and patents obtained with YFRF support

Patents

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